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OCT 25 2006

Amendments to the Specification

Please replace the paragraph at page 53, lines 10-28, with the following amended paragraph:

The symbols V_{0F}, V_{1F}, and V_{2F} are "jammed," meaning inputted at various locations, into the delay line 1504 of the DFE 612. Based on these symbols, the DFE 612 produces an intersymbol interference (ISI) replica portion associated with all previous symbols except the two most recent (since it was derived without using the first two taps of the DFE 612). The ISI replica portion represents a single-state ISI compensation signal. The ISI replica portion is subtracted form the output 37 of the deskew memory block 36 to produce the signal 1508 which is then fed to the MDFE block. The signal 1508 is denoted as the "tail" component in FIG. 3. In the illustrated embodiment, the DFE 612 has 33 taps, numbered from 0 through 32, and the tail component 1508 is associated with taps 2 through 32. As shown in FIG. 15, due to a circuit layout reason, the tail component 1508 is obtained in two steps. First, the ISI replica associated with taps 3 through 32 is subtracted from the deskew memory output 37 to produce an intermediate signal 1507. Then, the ISI replica associated with the tap 2 is subtracted from the intermediate signal 1507 to produce the tail component 1508.

Please replace paragraph at page 59, lines 23-31, with the following amended paragraph:

FIG. 15 only shows the select logic and the 25-to-1 multiplexer for one state and for one constituent transceiver. There are identical select logics and 25-to-1 multiplexers for the eight states and for each constituent transceiver. In other words, the computation of the 25 values is done only once for all the eight states, but the 25:1 MUX and the select logic are replicated eight times, one for each state. The input 614 to the Viterbi decoder 604 is, as a practical matter, eight 4D Viterbi inputs. Therefore, the output of the MDFE 602 is an 8-state representation signal. More generally, in a system utilizing N states, the output of the MDFE 602 is an N-state representation signal. Because the MDFE 602 produces an N-state representation signal based on a single-state ISI compensation signal, the MDFE can be referred to as a state multiplication circuit.

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